AMENDMENTS TO THE SUBSTITUTE SPECIFICATION

In the title:

Please change the title to read as follows:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING TEST CIRCUIT

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Please substitute the following paragraph for the paragraph beginning at line 9:

In the normal operation mode, as described above, when the clock pulse CLK is high, the output of the NAND gate goes low, to turn on the CMOS switch (Q1 and Q2) and to turn off the CMOS switch (Q3 and Q4) so that the read out signal from the memory cell is transferred as the output signal, Dout, through the main path made of inverters N1 and N2. When the clock pulse CLK goes from high to low, the output signal of the NAND gate G1 goes high, turning off the CMOS switch (Q1 and Q2), and turning ~~off~~ on the CMOS switch (Q3 and Q4). As a result, a feedback loop is formed so as to hold the read out signal from the memory cell in the latch of the inverters N1 and N2.

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Please substitute the following paragraph for the paragraph beginning at line 20:

A circuit for receiving scan data at the time of test includes the following components and is provided in the feedback loop of the first latch. The scan in signal Sin is fed to the input of a clocked inverter CN2. The output signal of the clocked inverter CN2 is transferred through a CMOS switch having a p-channel MOSFET ~~Q17~~ Q19 and an n-channel MOSFET ~~Q18~~ Q20 to the node between the output of the clocked inverter CN1 of the feedback loop and the CMOS switch (Q13 and Q14). There is also provided an inverter N18 for forming scan out signal Sout upon reception of the output from the inverter N12 of the second latch.

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Please substitute the following paragraph for the paragraph beginning at line 16:

In the test mode operation as described above, if the clock pulse CLK is low, the output of the inverter N16 goes high and the output of the inverter N17 goes low. The low signal of the inverter N17 causes the clocked inverter CN1 in the feedback loop of the first latch to be high-impedance output, and the CMOS switch (Q19 and Q20) for test signal

selection to be turned on. In the first latch, the scan in signal Sin is introduced, wherein the scan in signal Sin having passed through the clocked inverter ~~CN12~~ CN2 is input from the feedback loop via the CMOS switch (Q13 and Q14) that is on, to feed to the input of the inverter N11 in the main path.

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Please substitute the following paragraph for the paragraph beginning at line 12:

When the clock pulse CLK goes from low to high, the CMOS switch (Q19 and Q20) for the test signal selection in the first latch is turned off activating the clocked inverter CN1. This creates the feedback loop to form a latch between the inverter ~~N1~~ N11 and the clocked inverter CN1 to retain the previously obtained scan in signal Sin.